Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. (canceled)

9. (original) A fabrication process for making an enhanced avalanche ruggedness Fast Recovery Diode, the process comprising:

selecting a semiconductor material of a first dopant type;

patterning and introducing a first dopant of a second type opposite in polarity to the first dopant type into the top surface of the semiconductor material at a peripheral region of the device;

diffusing said first dopant to create field spreading structures for blocking reverse voltage;

introducing a second dopant of the first type into a central portion of the semiconductor material top surface;

diffusing said second dopant to create a region with enhanced doping concentration of the first type within the semiconductor material in the central portion of the device;

introducing and diffusing a third dopant of the second type to a predetermined depth within said enhanced doping region to form a main PN junction and effect a lower avalanche breakdown in the central portion in relationship to a periphery of the main PN junction; and

completing the device by forming metal electrodes on the top surface and a backside of the semiconductor material to conduct current through the diode.

10. (original) A fabrication process according to claim 9 wherein the concentration of the second dopant of the first type is in the range of 1.0E15 to 5.0E17 /cm3 and a diffusion depth of 3 to10 um.

11. (original) A fabrication process according to claim 9 wherein the concentration of the third dopant of the second type is in the range of 1.0E16 to 5.0E18 /cm3 and a diffusion depth of 2 to 6 um.

12. (original) A fabrication process according to claim 9 wherein the amount of additional charge contained between the second dopant of the first type and the starting epitaxial layer is in the range of 1.0E11 to 1.0E13 /cm2.

13. (original) A fabrication process according to claim 9 including introducing and diffusing life-time control dopant into the semiconductor to control device speed.

14. (original) A fabrication process for making an enhanced avalanche ruggedness Fast Recovery Diode comprising:

selecting a semiconductor material of a first dopant type;

patterning and defining a field spreading region and a central conduction region of the diode in a top surface of the semiconductor material;

patterning and defining within the central conduction region trenches of a predetermined depth in the semiconductor material;

introducing and diffusing a first dopant of a second type opposite in polarity to the dopant of the first type into the top surface in said defined field spreading region and central conduction region, said diffusion creating in the central conduction region a PN junction having acute curvature at the corners and edges of said trenches; and

completing the device by forming metal electrodes on the frontside and backside of the semiconductor to conduct current through the device.

15. (original) A fabrication process according to claim 14 in which the diffusion has a depth that is greater than one half the trench depth to form a PN diode wherein the P-diffusions originating at two height levels spaced apart by the depth of the trench are linked.

16. (original) A fabrication process according to claim 14 in which the diffusion has a depth which is shallower than one half the trench depth to create a merged Schottky-PIN structure.

17. (currently amended) A fabrication process according to claim ~~14 in which~~ 9, including introducing and diffusing life-time control dopant into the semiconductor to control device speed.

18. (original) A fabrication process for making an enhanced avalanche ruggedness Fast Recovery Diode comprising:

selecting a semiconductor material of a first dopant type;

patterning and defining a central conduction region bounded by a periphery in a top surface of the semiconductor material;

etching to reduce the semiconductor material thickness by about 15 to 20% within said defined central conduction region in relationship to its periphery;

patterning and defining a field spreading region surrounding the central conduction region of the device;

introducing and diffusing a first dopant of a second type opposite in polarity to the dopant of the first type into the top surface in said defined field spreading region and central conduction region; and

completing the device by forming metal electrodes on the frontside and backside of the semiconductor to conduct current through the device.

19. (original) A fabrication process according to claim 18 including introducing and diffusing life-time control dopant into the semiconductor to control device speed.

20. (currently amended) The fabrication process according to any of claims 9, 14 and 18 further comprising a blanket implant of the first dopant type into the semiconductor surface to counter the effect of counter-doping and compensation by ~~the~~ a life-time control dopant.

21. (original) The fabrication process according to any of claims 9, 14 and 18 in which the semiconductor material comprises a lightly doped epitaxial layer on top of a heavily doped substrate.

22. (original) The fabrication process according to any of claims 9, 14 and 18 further comprising a first deep life-time control dopant profile having a gradient that is higher

in doping concentration toward the backside of the semiconductor; and

a second shallow life-time control profile having a gradient that is heavier toward the top surface forming a shallow gradient band of decreasing concentration near the PN junction.

23. (original) The fabrication process according to claim 17 further comprising a first deep life-time control dopant profile having a gradient that is higher in doping concentration toward the backside of the semiconductor; and

a second shallow life-time control profile having a gradient that is heavier toward the top surface forming a shallow gradient band of decreasing concentration near the PN junction.

24. (currently amended) ~~The method of creating large area avalanche breakdown~~ A fabrication process according to ~~claim 17~~ any of claims 9, 17, 26 and 27 wherein the PN junction is formed by a body diffusion of a MOS gate-controlled device.

25. (currently amended) ~~The method of creating large area avalanche~~ A fabrication process according to ~~claim 17~~ any of claims 9, 17, 26 and 27 wherein the PN junction is the deeply placed P+ diffusion underneath a ~~trench~~ body diffusion in a MOS gate-controlled device.

26. (new) A fabrication process according to claim 9 including irradiating the semiconductor to effect a life-time control to control device speed.

27. (new) A fabrication process according to claim 9 including introducing a preliminary dopant of the first type prior to the step of patterning and introducing the first dopant of the second type to prevent current flow along a surface of the semiconductor material between an active area and an edge of the device across the field-spreading structures.